Abstract of the Disclosure:

In a semiconductor memory, there is capacitive coupling between bit lines that largely run in parallel. Outer sections of the bit lines are connected via respective switches to a sense amplifier arranged between the switches. When a memory cell is being read, the capacitive interference by other bit lines that are not coupled to the memory cell being read is kept as low as possible before the start of amplification by the sense amplifier by turning on the switches in that bit line. During the amplification phase, the remote outer section of that bit line is disconnected using the appropriate switch. In one embodiment, the capacitance of the bit line that is not connected to the memory cell to be read is increased further by additionally activating a precharging circuit.

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